CLAIMS

What is claimed is:

1. A processor, comprising:

circuit to receive a macro instruction specifying an operation, and specifying a first and a second data operand in first and second registers, respectively; and

one or more execution units to split the macro instruction into a first micro instruction and a second micro instruction, the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a first portion of the second data operand, and the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand, and to execute the first micro instruction, and to execute the second micro instruction.

2. The processor of claim 1, wherein the execution of the first micro instruction is performed during a first clock cycle.

3. The processor of claim 1, wherein the execution of the second micro instruction is performed during a subsequent clock cycle.

4. The processor of claim 1, wherein the execution of the first micro instruction is performed during a first half clock cycle.

5. The processor of claim 1, wherein the execution of the second micro instruction is performed during a second half clock cycle.

6. The processor of claim 1, further comprises a register file coupled with the circuit, the register file having a third data operand including a plurality of data elements corresponding to the first data operand and the second data operand.

7. The processor of claim 6, wherein the plurality of data elements includes 128-bits of data from the register file.

8. A system, comprising:

a storage medium;

a processor coupled with the storage medium, the processor having

circuit to receive a macro instruction specifying an operation, and specifying a first and a second data operand in first and second registers, respectively, and

one or more execution units to split the macro instruction into a first micro instruction and a second micro instruction, the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a

first portion of the second data operand, and the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand, and to execute the first micro instruction, and to execute the second micro instruction; and

a register file coupled with the processor, the register file having a third data operand including a plurality of data elements corresponding to the first data operand and the second data operand.

9. The system of claim 8, wherein the execution of the first micro instruction is performed during a first clock cycle, and the execution of the second micro instruction is performed during a second clock cycle.

10. The system of claim 8, wherein the execution of the first micro instruction is performed during a first half clock cycle, and execution of the second micro instruction is performed during a second half clock cycle.

11. A method, comprising:

receiving a macro instruction specifying an operation, and specifying a first and a second data operand in first and second registers, respectively; and

splitting the macro instruction into a first micro instruction and a second micro instruction, the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand

and a first portion of the second data operand, and the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand.

12. The method of claim 11, further comprising:

executing the first micro instruction; and

executing the second micro instruction.

13. The method of claim 12, wherein the execution of the first micro instruction is performed during a first clock cycle, and the execution of the second micro instruction is performed during a second clock cycle.

14. The method of claim 13, wherein the execution of the first micro instruction is performed during a first clock cycle, and the execution of the second micro instruction is performed during a second clock cycle.